Precision Measurement Central (4)

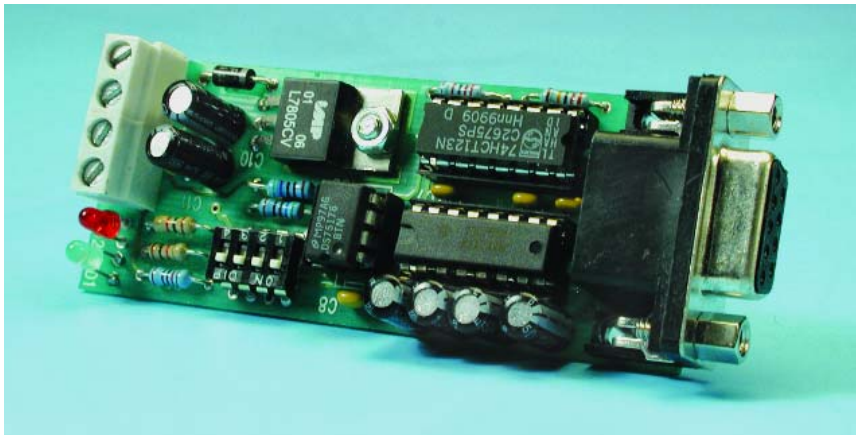
Part 4: RS485, or networking the MSC1210 micro

Design by J. Wickenhäuser

www.wickenhaeuser.com

The RS485 port on the MSC1210 board provides great opportunities for communication with other systems. For example, it allows a number of MSC1210 boards to be connected up into a network and talk to one another over distances of several kilometres.

This fourth instalment in the series on the MSC1210-based Precision Measurement Central (kicked off in the July/August 2003 issue) is entirely devoted to the RS485 interface. This month we will cover the theory and hardware. The December 2003 issue, finally, will discuss the practical use of the RS485 interface in a small project that goes to show how up to 255 MSC1210 boards can communicate with a single PC through an RS485 link. The converter required for the job is discussed in this article instalment.



RS485

Although the RS485 interface has been around virtually since the earliest days of the PC era, it is rarely seen in real life, that is, on the PC's connector panel. That's why we take this opportunity to present a suitable converter for RS232 to RS485, which has been tailored for use in combination with the MSC1210 board. First, however, we need to wade though some theory.

Bus topology

Normally an RS485 network consists of a long cable (bus) of which the ends are terminated with resistors. Up to 32 devices may be connected to the bus, or even 256 if a suitable driver chip is used. Ideally, all devices are connected to form a long thread. In practice, however, individual bus participants may also be connected via branches of several metres (**Figure 1**). In 'minimum' cases only the two wires designated 'A' and 'B' are required, although it is recommended to implement potential cancellation using a third wire and an optional resistor. Another popular variant has four wires and allows the devices to be powered over the bus.

The digital information conveyed over the RS485 bus comprises the voltage difference between line 'A' and 'B'. If the difference is positive, the bus is said to convey a logic 1. In the other case, a logic 0 is conveyed. The use of differential voltages makes the bus rather immune to noise, provided a number of conditions are satisfied. **Figure 2** shows a bus with two devices on it, where the signal is to be carried from IN to OUT over a long cable. An oscilloscope is connected to the bus at the indicated position. Any cable will have a more or less distinctive impedance — values of 60 to 200 Ω being typical. The signal on the cable will remain undistorted only if the cable is terminated with a resistor whose value is approximately equal to the cable impedance. Wrong termination values cause signal distortion that can lead to data corruption and increased susceptibility of the bus to noise.

Fortunately, correct cable termination is really critical only in those cases where signals with a high data rate (> 57,600 bits/s) are conveyed over cable lengths exceeding

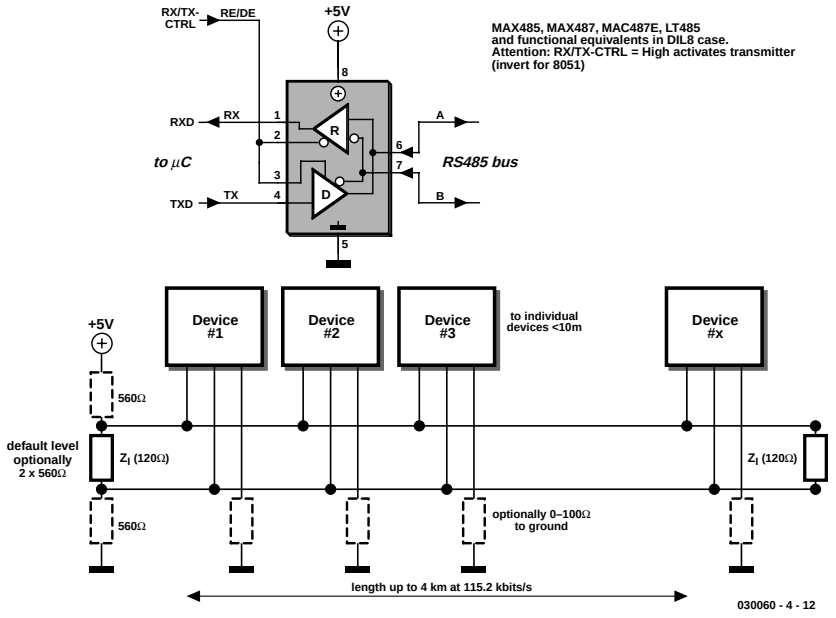


Figure 1. RS485 topology.

500 m, when the propagation times start to approach the bit rates (the signal travels 100-300 m in 1 µs). With cable lengths under 50 m and bit rates under 57,600, a cheap cable with no specified impedance but terminated with 120 Ω at both ends should be adequate.

Overvoltage Protection 'lite'

An RS485 driver must be capable of withstanding line voltages between –7 V and +12 V at its input(s). Fair enough, but longish cables in particular are prone to pick up (by induction) much higher peak voltages caused by electrostatic fields, discharges, EMI transients and so on. Consequently it makes sense to protect all RS485 against voltage surges. With suitable protection, short and not too powerful transients can not harm the drivers ICs (**Figure 3**).

Data traffic

The drawing in Figure 1 includes all optional resistors. These resistors serve to pull the bus to a fixed logic level when there is no traffic (that is, all devices are receiving and none is putting data on the bus). Unfortunately, this variant is rather wasteful in terms of energy usage and at the same time likely to cause problems with long cables.

A better alternative is shown in **Figure 4**. In this configuration, the initial level of the bus is not known. If a device wants to put a data block on the bus, it has to activate its transmitter section first. However, as a result of improper termination as illustrated in Figure 2, it may happen that activation of the transmitter alone is sufficient for receiving devices on the bus to recognise data, when in fact no valid data has been sent as yet (see block marked ???).

This leads to the absolute requirement for a pause to be inserted immediately after activation of each transmitter section. This 'dead' period needs to be much longer than prescribed for the transmission of a single byte (t_byte). The time needed to convey a byte over the bus is roughly ten times the reciprocal of the baud rate, or about 1 ms per byte when a rate of 9,600 bits/s is used.

The data packet proper always starts with a special marker byte (START). Note, however, that START may never occur within the actual data (more about this in the next instalment).

Because only one device can transmit at a time ('half duplex') a strict protocol is needed describing who's allowed to transmit what and when. If the protocol is not observed, data contention, collision and corruption is imminent. The practical application dis-

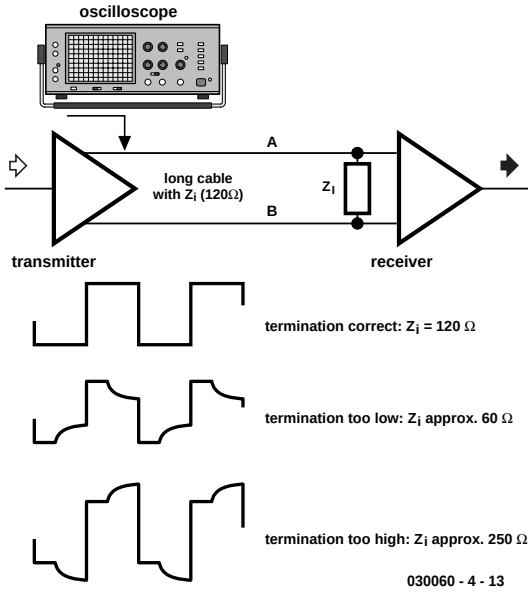


Figure 2. Why terminate?

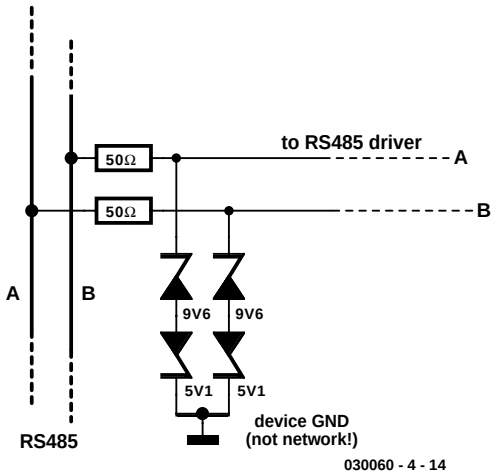


Figure 3. Surge protection by means of two zener diodes.

cussed in next month's instalment employs a simple but effective protocol.

A PC on the RS485 bus

If the two 560-Ω resistors shown in Figure 1 are used, the risk of 'undesired databytes' is greatly reduced. Problems may only occur with long cables (>50 m) and higher baud rates (>57,600 bits/s), particularly when the transmitting junction and the resistors are relatively far apart. Unfortunately, a PC can not exercise exact control over the pulse timing on its serial interface and so activate the transmitting device using an appropriate delay. After all, most PCs employ a UART (RS232 driver) with an internal transmitter FIFO. This prevents the PC from 'knowing' whether or not a databyte was actually sent or not. Consequently it is the task of the PC converter to ensure that the RS485 bus is at a valid logic level when there is no traffic.

The converter

The converter, of which the circuit diagram is given in **Figure** 5, operates largely as a 'dumb' extension which has the benefit of it supporting different protocols and, of course,

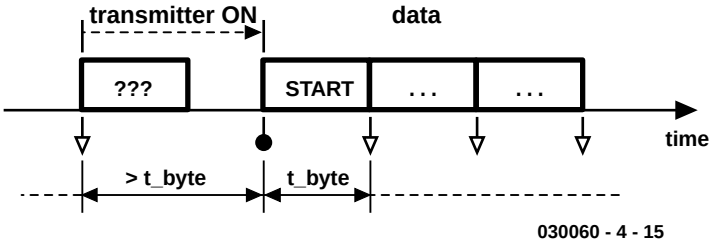


Figure 4. Transmit timing.

bit rates. The design consists of an RS232 and an RS485 converter separated by good old TTL levels.

Bits arriving at the RS485 bus are copied directly to the PC irrespective of the bit rate. Once the PC sends a character, the converter immediately switches on its transmitter via a retriggerable monostable (IC1.A). The transmitter remains active for the time its takes to convey the byte. In the case of our circuit, two times may be selected: 20 ms for 1200 bits/s (S1 opened) or 2 ms for 9600 bits/s and higher (S1 closed).

In addition, switch S1.4 may be used to include the terminator resistor, and/or S1.2/3 (operate at the same time) for the 560-Ω resistors to set the default level on the bus. These provisions on the converter allow several PCs or a combination of PCs and MSC1210 boards to be included in a network.

The construction of the converter on the printed circuit board shown in **Figure 6** should be an uncomplicated affair as there are no pitfalls with regard to soldering etc. The introductory photograph shows the author's prototype. The converter operates from an external supply voltage of

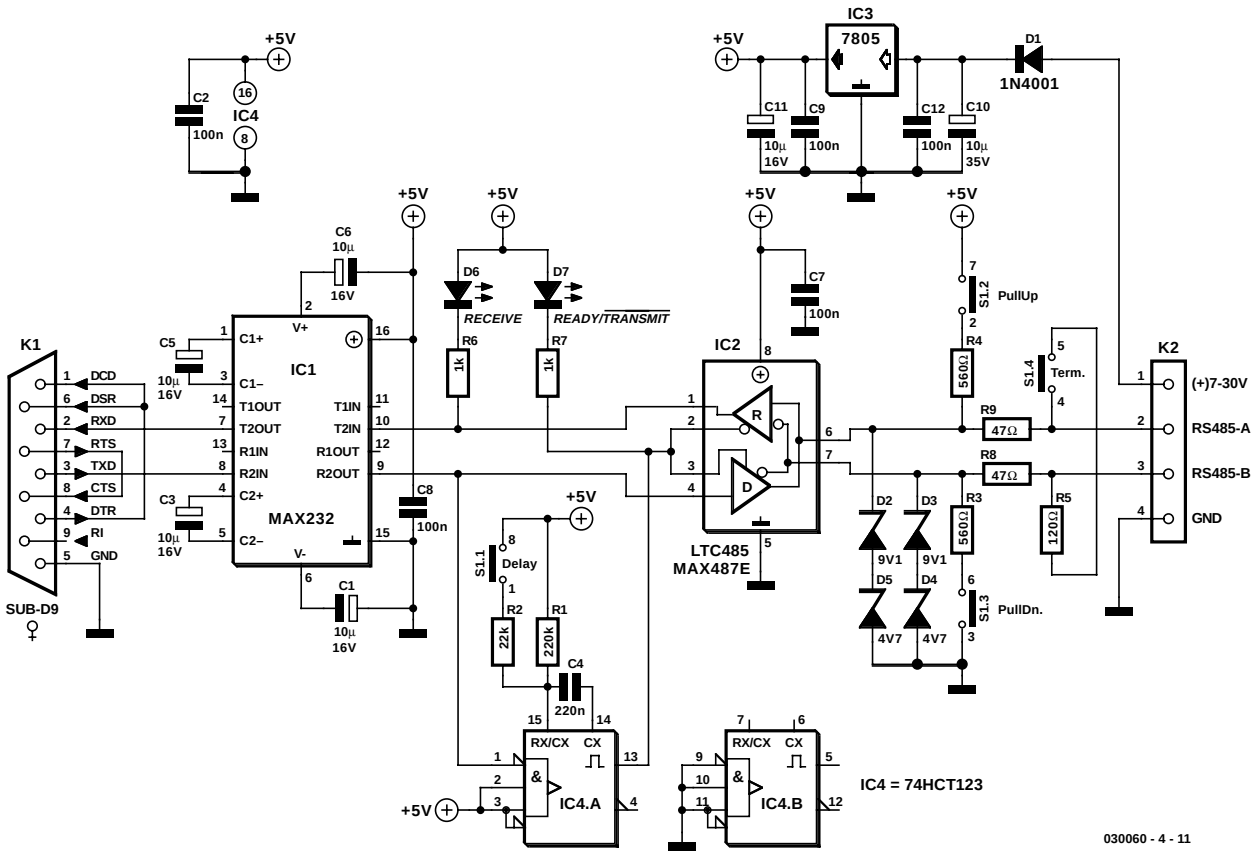


Figure 5. Circuit diagram of the RS232/RS485 converter.

COMPONENTS LIST

Resistors:
R1 = 220kΩ
R2 = 22kΩ
R3,R4 = 560Ω
R5 = 120Ω
R6,R7 = 1kΩ
R8,R9 = 47Ω

Capacitors:
C1,C3,C5,C6,C11 = 10µF 16V radial
C2,C7,C8,C9,C12 = 100nF
C4 = 220nF (10% tolerance)
C10 = 10µF 35V radial

Semiconductors:
D1 = 1N4001 (DO41 case)
D2,D3 = 9V1 zener diode
D4,D5 = 4V7 zener diode
D6 = LED, low current, green, 3mm
D7 = LED, low current, red, 3mm
IC1 = MAX232 (DIL case)
IC2 = LTC485 or MAX487E (ESD/EMI-optimised) (DIL case)
IC3 = 7805 (TO220 case)
IC4 = 74HCT123 (DIL case) (Philips preferred)

Miscellaneous:
K1 = 9-way sub-D socket, PCB mount, angled pins
K2 = 4-way PCB terminal block, 5mm lead pitch
S1 = 4-way DIL switch

between 7 V and 30 V and draws a modest 20 mA or so. In case the supply voltage is not obtained from the bus, the RS485 ground is connected to the circuit ground using a 100-Ω resistor for potential equalisation.

(030060-4)

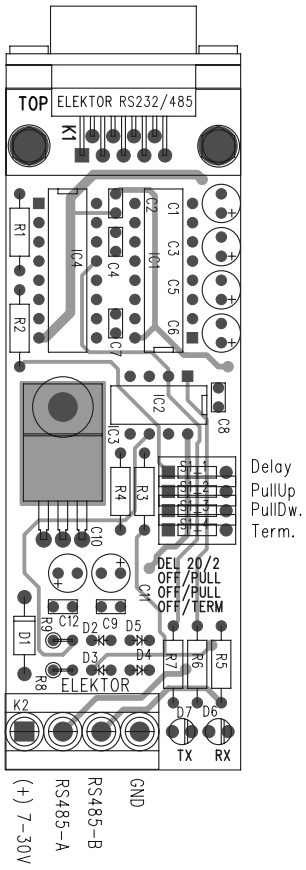
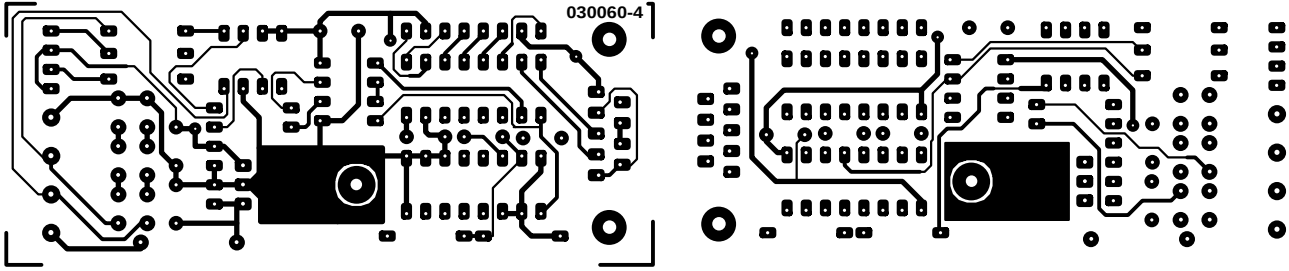
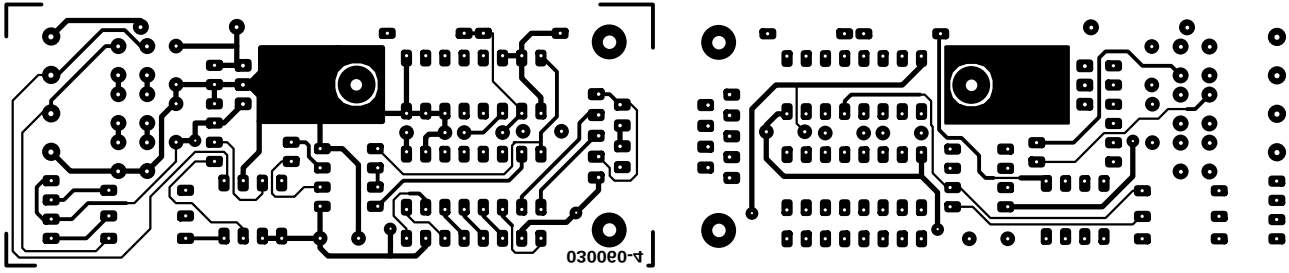


Figure 6. PCB design for the RS232/RS485 converter.



non reflected

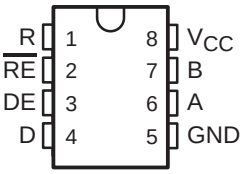


reflected

SLLS101B – JULY 1985 – REVISED JUNE 1999

- **Bidirectional Transceivers**
- **Meet or Exceed the Requirements of ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Driver and Receiver Outputs**
- **Individual Driver and Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capability . . . ±60 mA Max**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operate From Single 5-V Supply**

D OR P PACKAGE
(TOP VIEW)



description

The SN65176B and SN75176B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN65176B is characterized for operation from –40°C to 105°C and the SN75176B is characterized for operation from 0°C to 70°C.

Function Tables

DRIVER

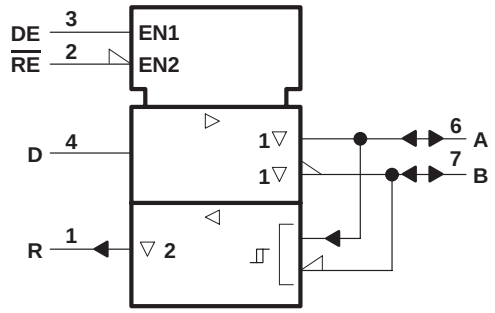
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	?

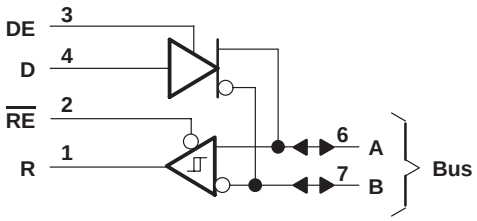
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†

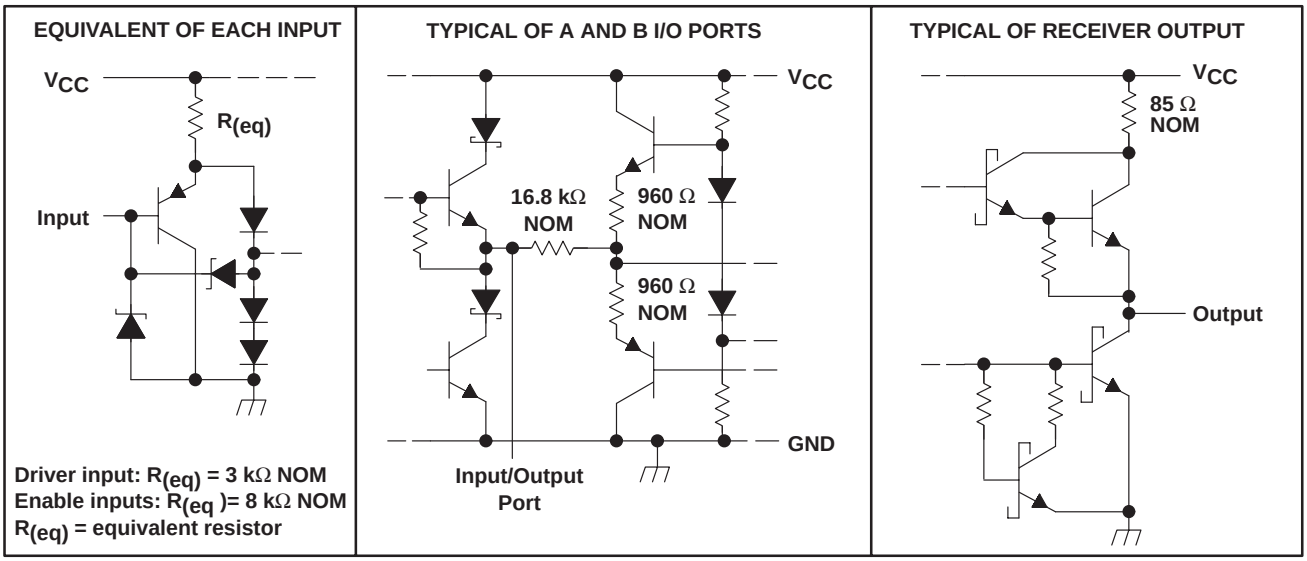


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage range at any bus terminal . . . . . –10 V to 15 V
Enable input voltage, V_I . . . . . 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 197°C/W
P package . . . . . 104°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				–7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 3)				±12	V
High-level output current, I_{OH}	Driver			–60	mA
	Receiver			–400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65176B	–40		105	°C
	SN75176B	0		70	

NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5	3.6	6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		1/2 V_{OD1} or 2¶			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 4		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					+3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 5	V_O = 12 V			1	mA
			V_O = – 7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current	V_O = –7 V				–250	mA
		V_O = 0				150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

† The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
NOTES: 4. See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.
5. This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics, V_{CC} = 5 V, R_L = 110 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω, See Figure 3			15	22	ns
$t_{t(OD)}$	Differential-output transition time				20	30	ns
t_{PZH}	Output enable time to high level	See Figure 4			85	120	ns
t_{PZL}	Output enable time to low level	See Figure 5			40	60	ns
t_{PHZ}	Output disable time from high level	See Figure 4			150	250	ns
t_{PLZ}	Output disable time from low level	See Figure 5			20	30	ns

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\ \|V_t\| - \|\overline{V}_t\|\ \|$	$\|\ \|V_t - \|\overline{V}_t\|\ \|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 6	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				−100	μA
r_I	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 6: This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V, See Figure 6		21	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			23	35	ns
t_{PZH}	Output enable time to high level	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	ns
t_{PHZ}	Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

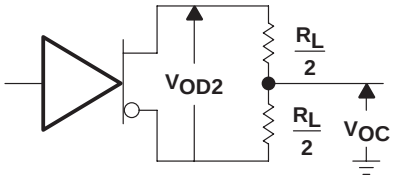


Figure 1. Driver V_{OD} and V_{OC}

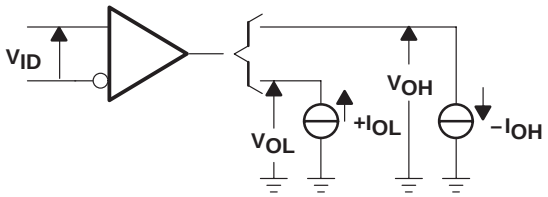
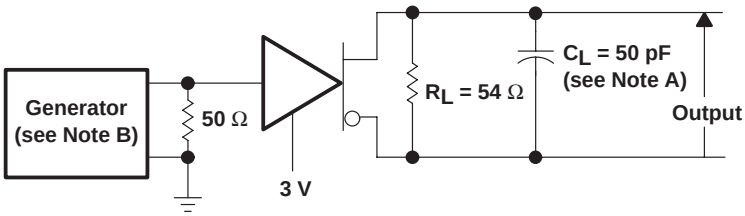
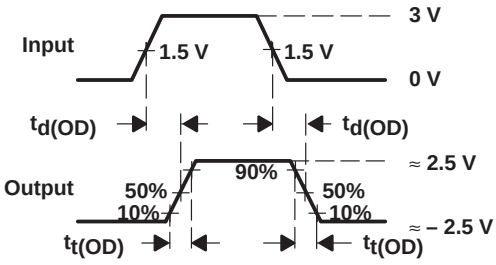


Figure 2. Receiver V_{OH} and V_{OL}



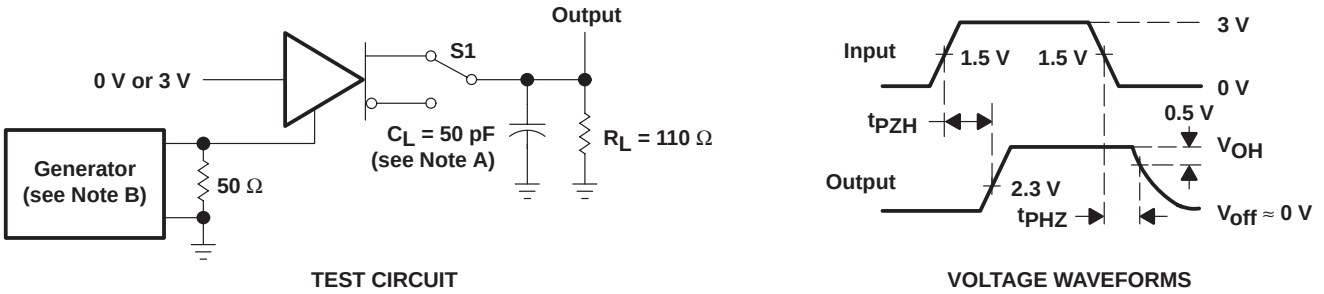
TEST CIRCUIT



VOLTAGE WAVEFORMS

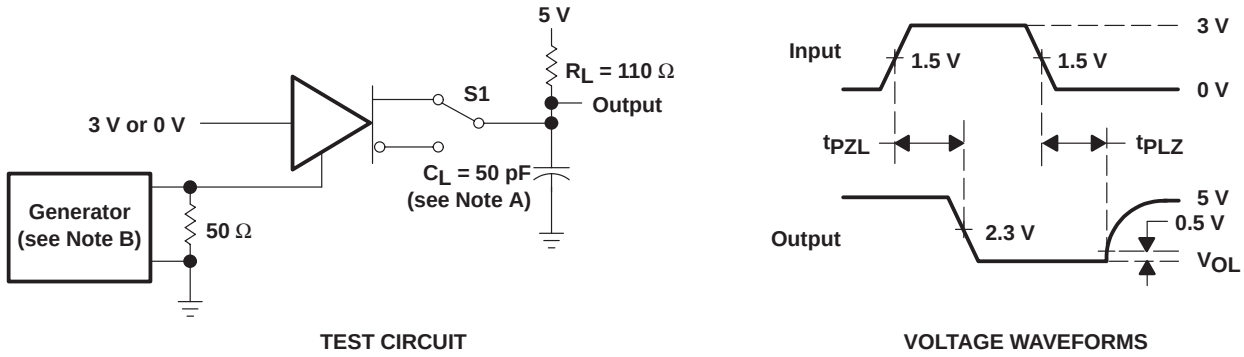
NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 3. Driver Test Circuit and Voltage Waveforms



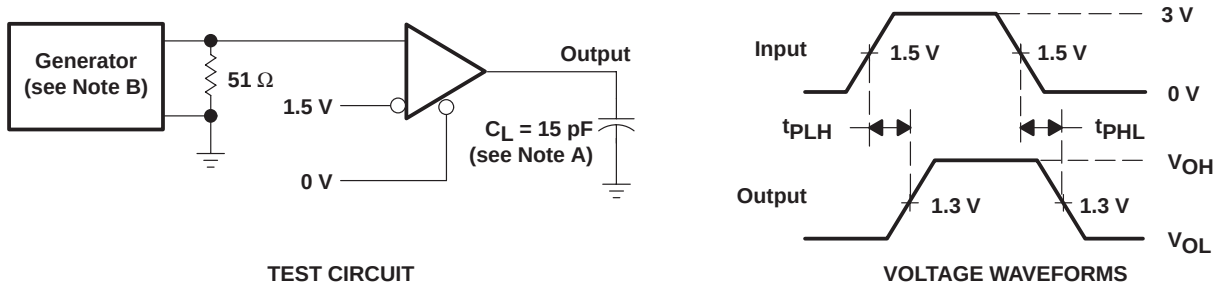
NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 4. Driver Test Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

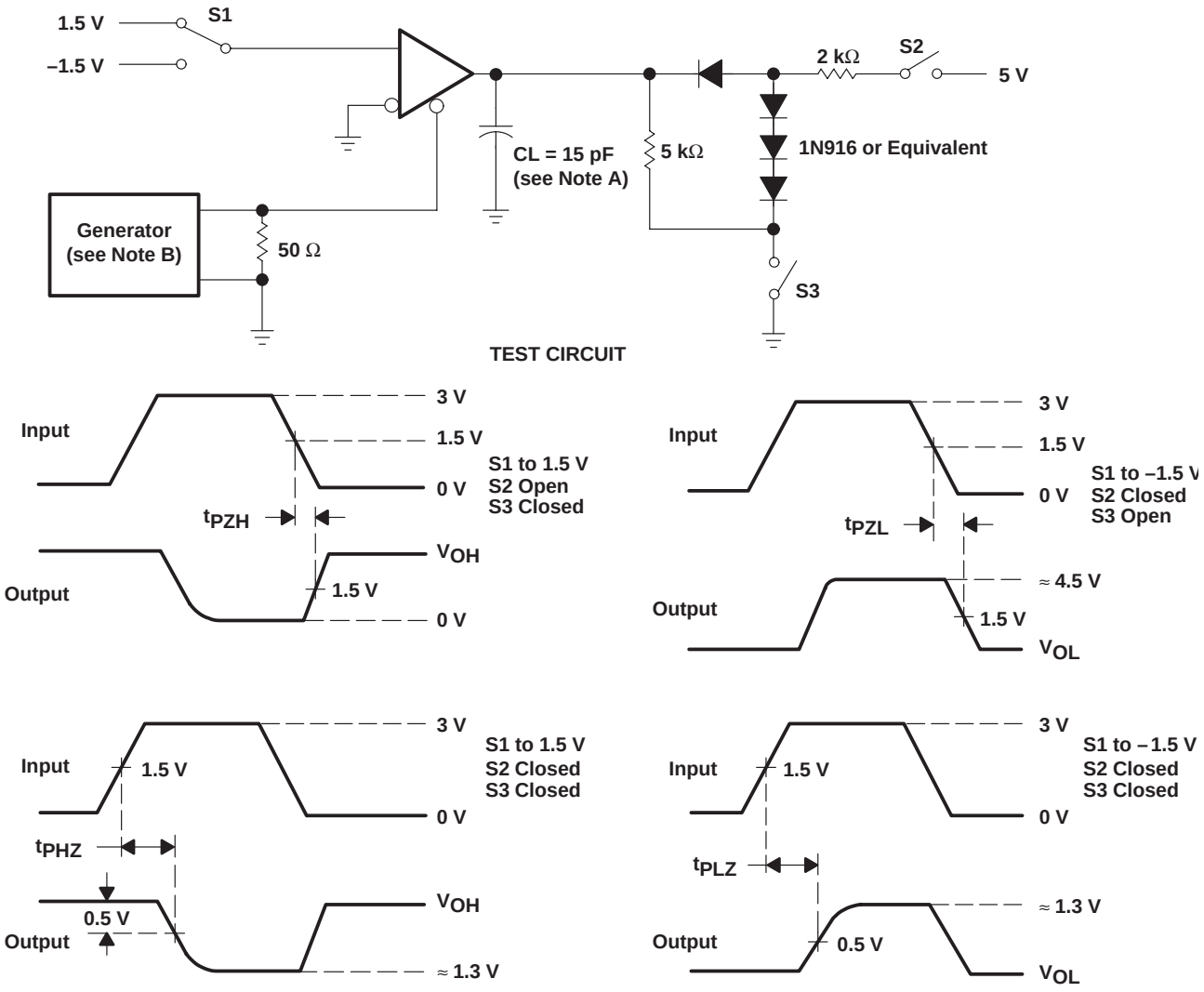
Figure 5. Driver Test Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 6. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

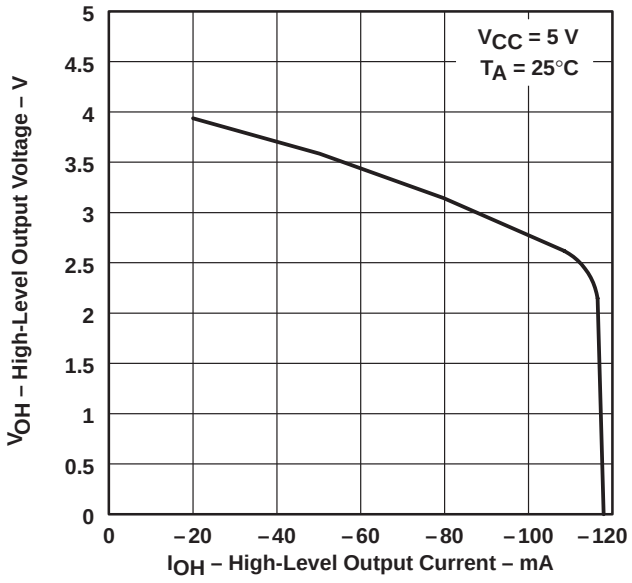


Figure 8

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

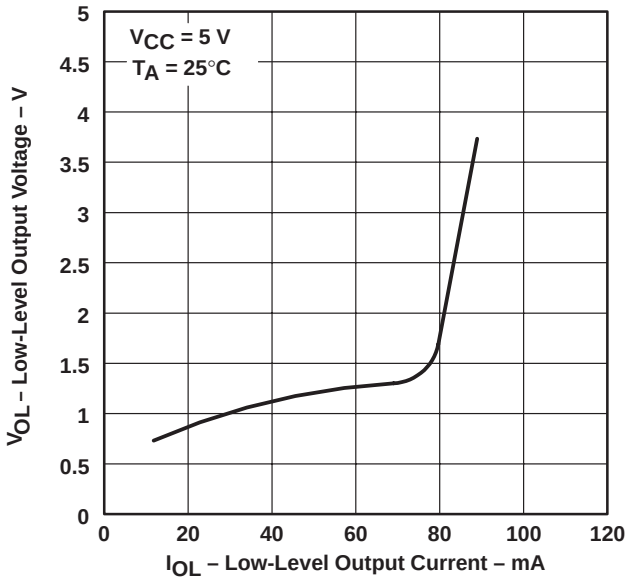


Figure 9

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

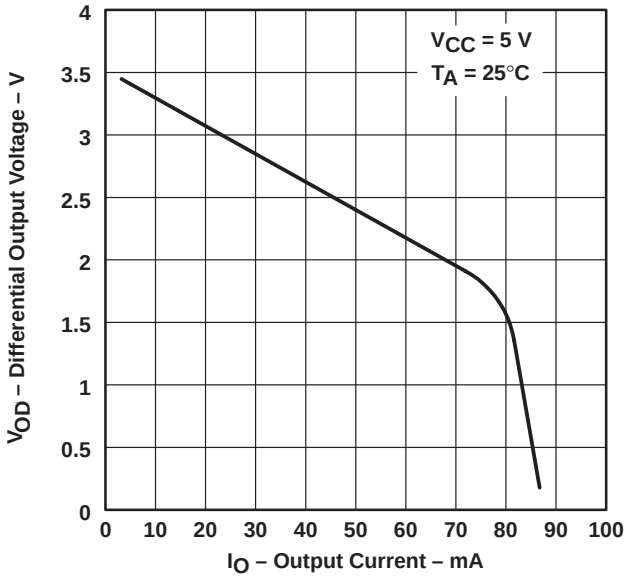


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

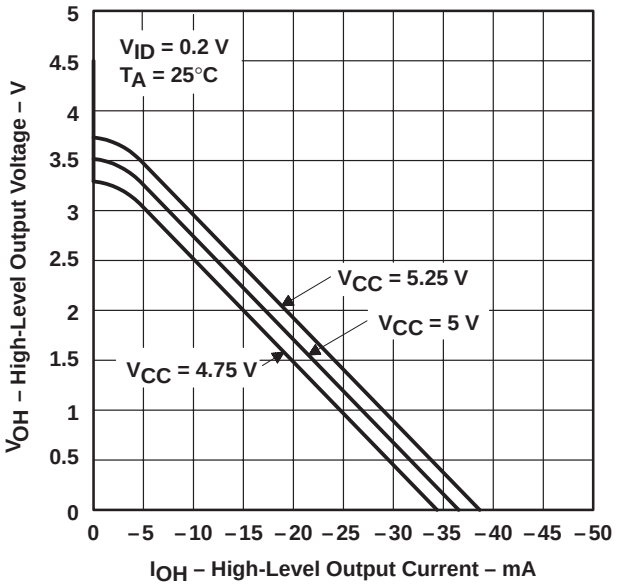
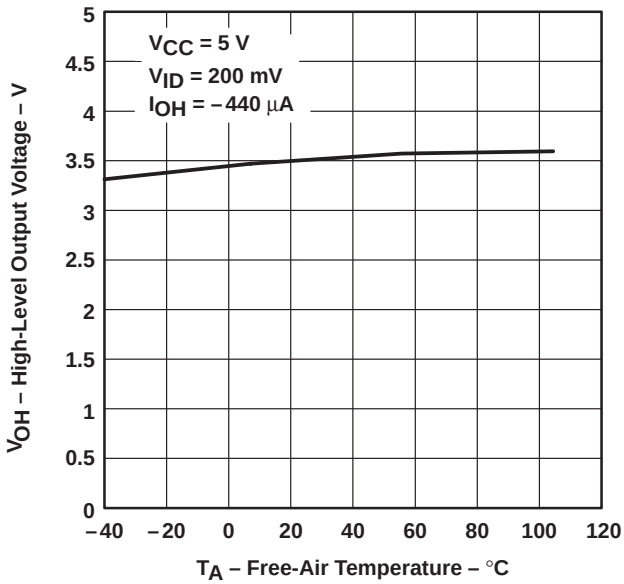


Figure 11

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†



† Only the 0°C to 70°C portion of the curve applies to the SN75176B.

Figure 12

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

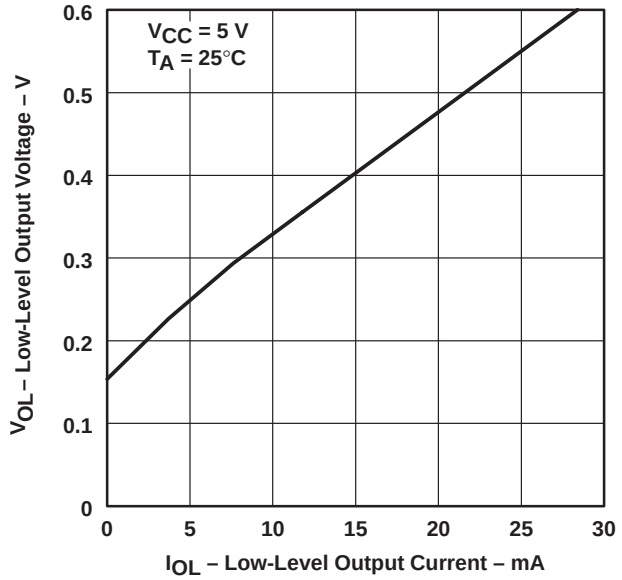


Figure 13

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

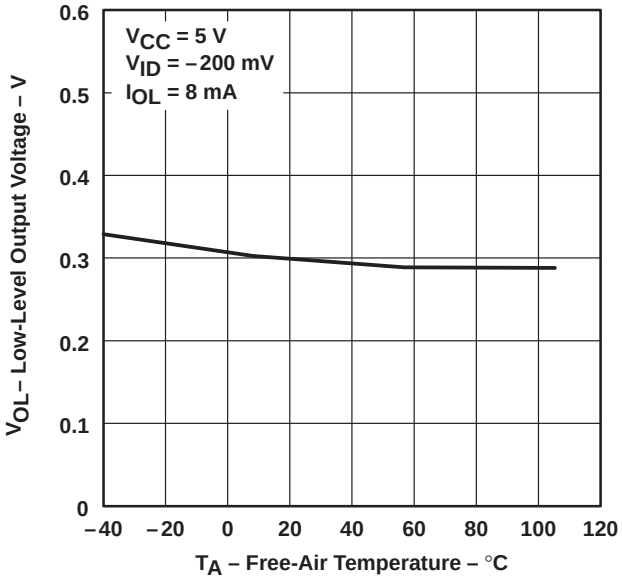


Figure 14

TYPICAL CHARACTERISTICS

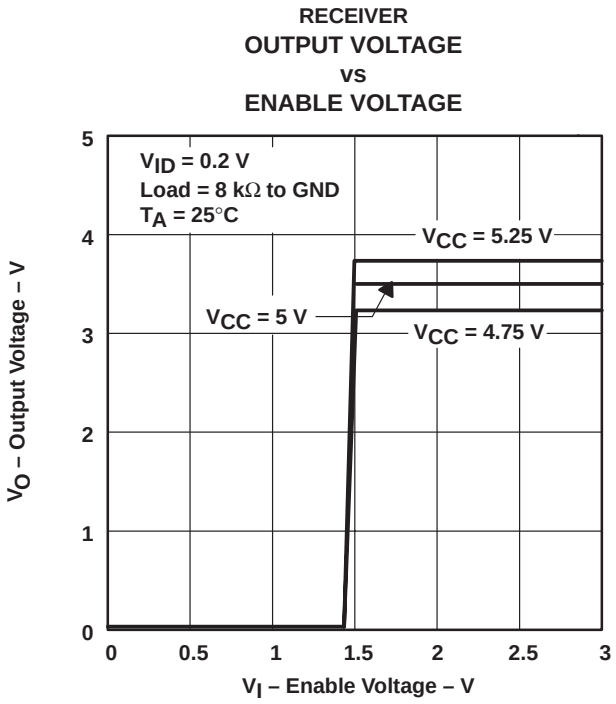


Figure 15

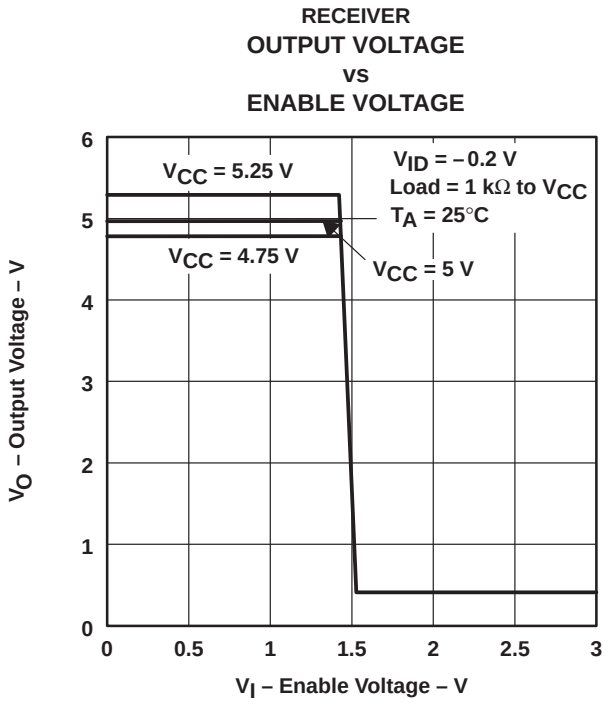
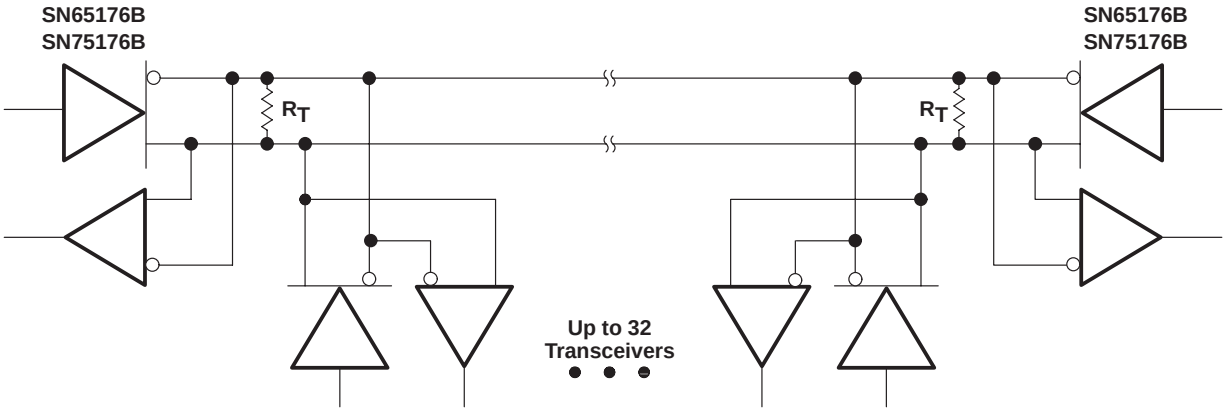


Figure 16

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 17. Typical Application Circuit

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.